DUAL H-BRIDGE MOTOR DRIVER

Check for Samples: DRV8833

FEATURES

- **Dual-H-Bridge Current-Control Motor Driver**
  - **Capable of Driving Two DC Motors or One Stepper Motor**
  - **Low MOSFET On-Resistance: HS + LS 360 mΩ**
- **Output Current (at V_M = 5 V, 25°C)**
  - **1.5-A RMS, 2-A Peak per H-Bridge in PWP and RTY Package Options**
  - **500-mA RMS, 2-A Peak per H-Bridge in PW Package Option**
- **Outputs Can Be Paralleled for**
  - **3-A RMS, 4-A Peak (PWP and RTY)**
  - **1-A RMS, 4-A Peak (PW)**
- **Wide Power Supply Voltage Range: 2.7 V – 10.8 V**
- **PWM Winding Current Regulation/Limiting**
- **Thermally Enhanced Surface Mount Packages (PWP and RTY)**

APPLICATIONS

- **Battery-Powered Toys**
- **POS Printers**
- **Video Security Cameras**
- **Office Automation Machines**
- **Gaming Machines**
- **Robotics**

DESCRIPTION

The DRV8833 provides a dual bridge motor driver solution for toys, printers, and other mechatronic applications.

The device has two H-bridge drivers, and can drive two DC brush motors, a bipolar stepper motor, solenoids, or other inductive loads.

The output driver block of each H-bridge consists of N-channel power MOSFET's configured as an H-bridge to drive the motor windings. Each H-bridge includes circuitry to regulate or limit the winding current.

Internal shutdown functions with a fault output pin are provided for over current protection, short circuit protection, under voltage lockout and overtemperature. A low-power sleep mode is also provided.

The DRV8833 is packaged in a 16-pin HTSSOP or QFN package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br) as well as a 16-pin TSSOP package.

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
PowerPAD™ (HTSSOP) - PWP	Reel of 2000	DRV8833PWPR	DRV8833
	Tube of 90	DRV8833PWP	
(TSSOP) - PW	Reel of 2000	DRV8833PWR	8833PW
	Tube of 90	DRV8833PW	
PowerPAD™ (QFN) - RTY	Reel of 3000	DRV8833RTYR	DRV8833
	Reel of 250	DRV8833RTYT	

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

Functional Block Diagram

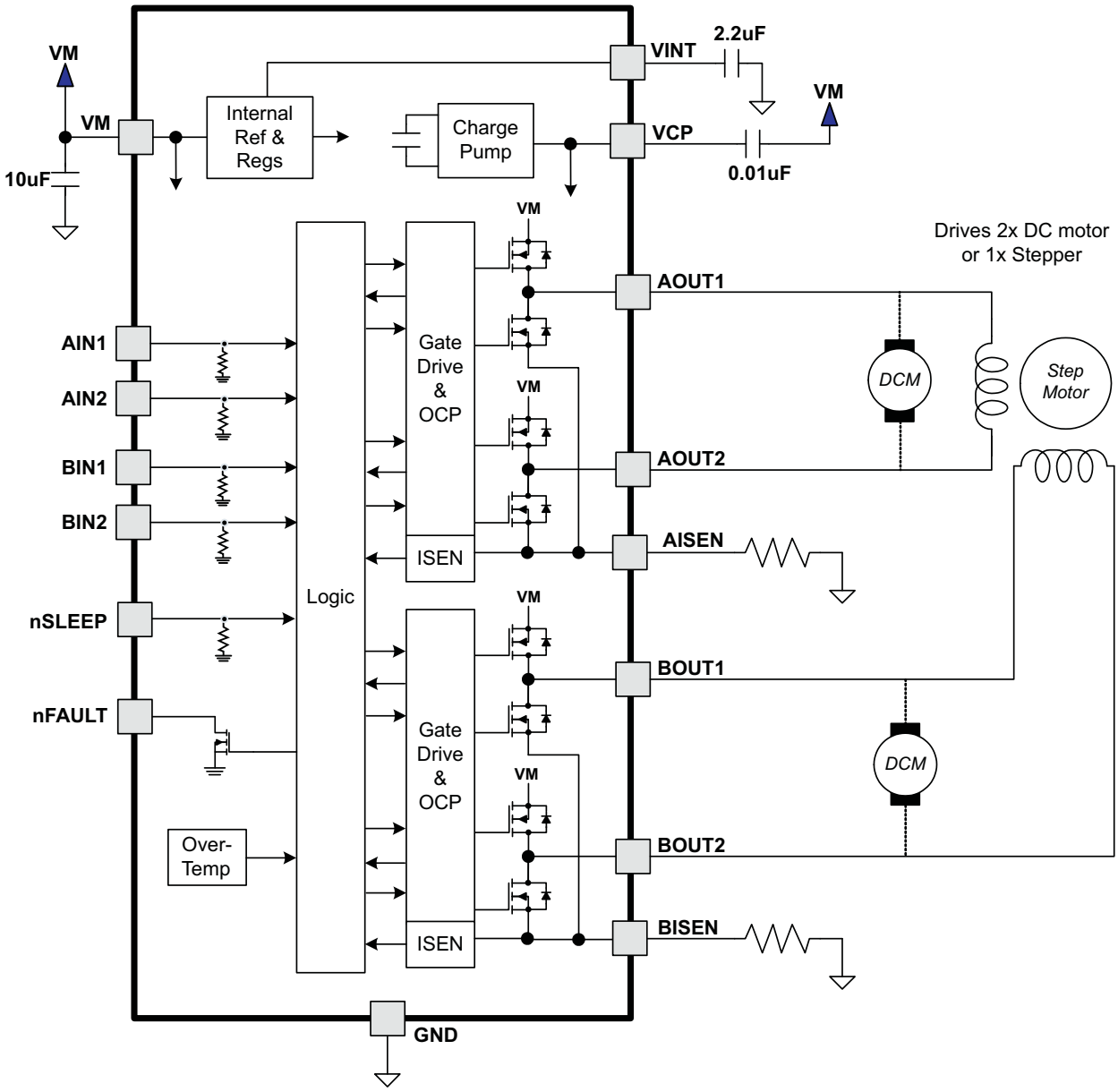
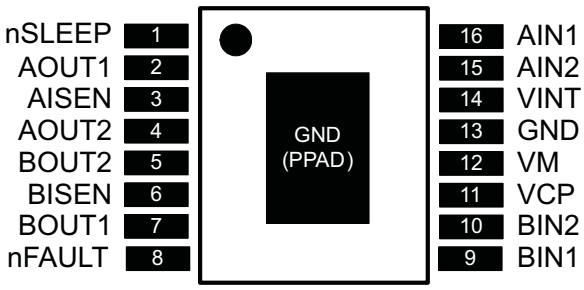


Table 1. TERMINAL FUNCTIONS

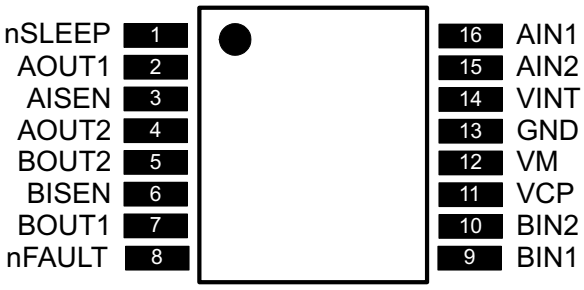
NAME	PIN (PWP or PW)	PIN (RTY)	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND					
GND	13 PPAD (PWP only)	11 PPAD	-	Device ground	Both the GND pin and device PowerPAD must be connected to ground
VM	12	10	-	Device power supply	Connect to motor supply. A 10-µF (minimum) ceramic bypass capacitor to GND is recommended.
VINT	14	12	-	Internal supply bypass	Bypass to GND with 2.2-µF, 6.3-V capacitor
VCP	11	9	IO	High-side gate drive voltage	Connect a 0.01-µF, 16-V (minimum) X7R ceramic capacitor to VM
CONTROL					
AIN1	16	14	I	Bridge A input 1	Logic input controls state of AOUT1. Internal pulldown.
AIN2	15	13	I	Bridge A input 2	Logic input controls state of AOUT2. Internal pulldown.
BIN1	9	7	I	Bridge B input 1	Logic input controls state of BOUT1. Internal pulldown.
BIN2	10	8	I	Bridge B input 2	Logic input controls state of BOUT2. Internal pulldown.
nSLEEP	1	15	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode and reset all internal logic. Internal pulldown.
STATUS					
nFAULT	8	6	OD	Fault output	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT					
AISEN	3	1	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A, or GND if current control not needed
BISEN	6	4	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B, or GND if current control not needed
AOUT1	2	16	O	Bridge A output 1	Connect to motor winding A
AOUT2	4	2	O	Bridge A output 2	
BOUT1	7	5	O	Bridge B output 1	Connect to motor winding B
BOUT2	5	3	O	Bridge B output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

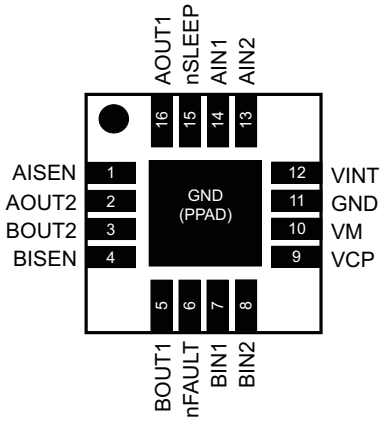
PWP PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



RTY PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 11.8	V
	Digital input pin voltage range	–0.5 to 7	V
	xISEN pin voltage	–0.3 to 0.5	V
	Peak motor drive output current	Internally limited	A
T_J	Operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC		PWP	RTY	PW	UNITS
		16 PINS	16 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	40.5	37.2	103.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	32.9	34.3	38	
θ_{JB}	Junction-to-board thermal resistance(3)	28.8	15.3	48.1	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.6	0.3	3	
ψ_{JB}	Junction-to-board characterization parameter(5)	11.5	15.4	47.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	4.8	3.5	N/A	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	2.7		10.8	V
V_{DIGIN}	Digital input pin voltage range	-0.3		5.75	V
I_{OUT}	PWP and RTY package continuous RMS or DC output current per bridge(2)			1.5	A
	PW package continuous RMS or DC output current per bridge(2)			0.5	

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) V_M = 5 V, power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	V_M = 5 V, xIN1 = 0 V, xIN2 = 0 V		1.7	3	mA
I_{VMQ}	VM sleep mode supply current	V_M = 5 V		1.6	2.5	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M falling			2.6	V
V_{HYS}	VM undervoltage lockout hysteresis			90		mV
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage	nSLEEP			0.5	V
		All other pins			0.7	
V_{IH}	Input high voltage	nSLEEP	2.5			V
		All other pins	2			
V_{HYS}	Input hysteresis			0.4		V
R_{PD}	Input pull-down resistance	nSLEEP		500		kΩ
		All except nSLEEP		150		
I_{IL}	Input low current	VIN = 0			1	µA
I_{IH}	Input high current	VIN = 3.3 V, nSLEEP		6.6	13	µA
		VIN = 3.3 V, all except nSLEEP		16.5	33	
t_{DEG}	Input deglitch time			450		ns
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		200		mΩ
		V_M = 5 V, I_O = 500 mA, T_J = 85°C			325	
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		250		
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C			350	
	LS FET on resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		160		
		V_M = 5 V, I_O = 500 mA, T_J = 85°C			275	
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		200		
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C			300	
I_{OFF}	Off-state leakage current	V_M = 5 V, T_J = 25°C, V_{OUT} = 0 V	–1		1	µA
MOTOR DRIVER						
f_{PWM}	Current control PWM frequency	Internal PWM frequency		50		kHz
t_R	Rise time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		180		ns
t_F	Fall time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		160		ns
t_{PROP}	Propagation delay INx to OUTx	V_M = 5 V		1.1		µs
t_{DEAD}	Dead time (1)	V_M = 5 V		450		ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2	3.3		A
t_{DEG}	OCP Deglitch time			2.25		µs
t_{OCP}	Overcurrent protection period			1.35		ms
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

(1) Internal dead time. External implementation is not necessary.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONTROL						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{BLANK}	Current sense blanking time			3.75		µs
SLEEP MODE						
t_{WAKE}	Startup time	nSLEEP inactive high to H-bridge on			1	ms

FUNCTIONAL DESCRIPTION

PWM Motor Drivers

DRV8833 contains two identical H-bridge motor drivers with current-control PWM circuitry. A block diagram of the circuitry is shown below:

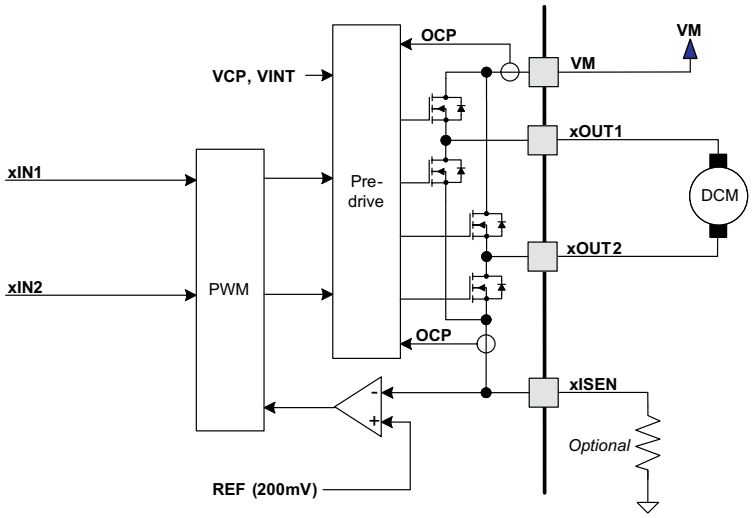


Figure 1. Motor Control Circuitry

Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs. Table 2 shows the logic.

Table 2. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to one xIN pin while the other is held low; to use slow decay, one xIN pin is held high.

Table 3. PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

Figure 2 shows the current paths in different drive and decay modes.

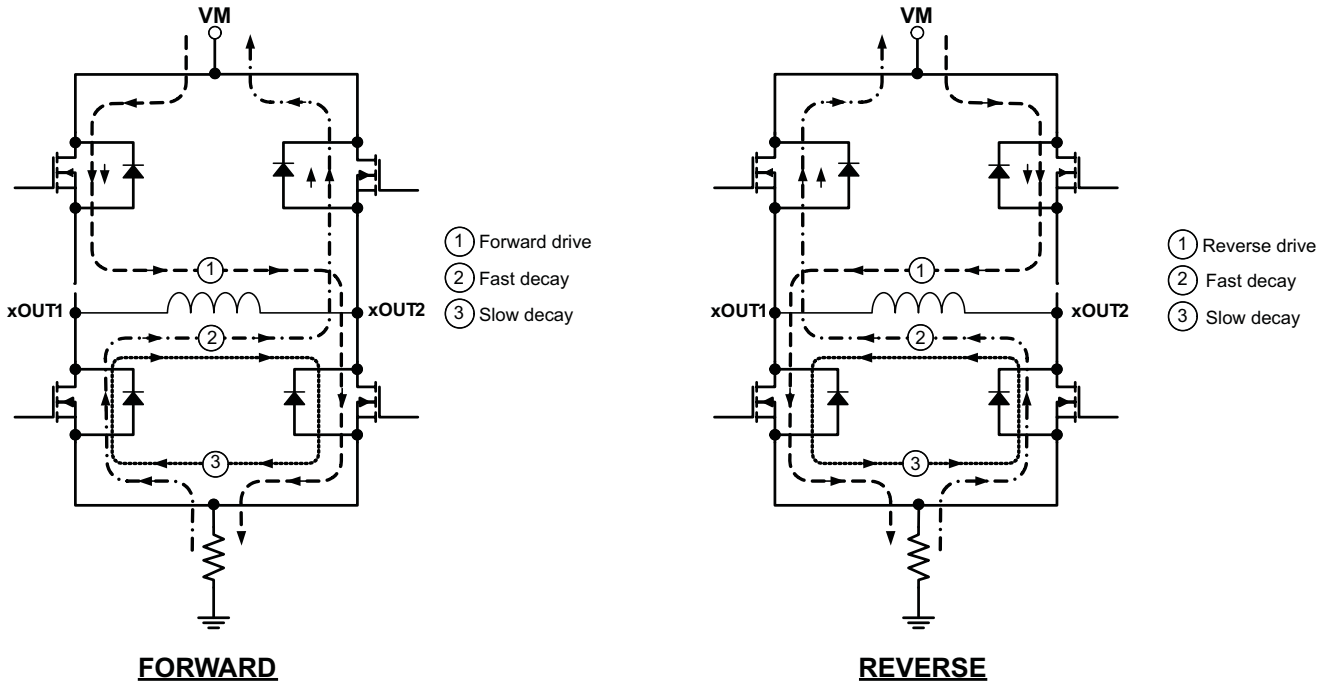


Figure 2. Decay Modes

Current Control

The current through the motor windings may be limited, or controlled, by a fixed-frequency PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage is fixed at 200 mV.

The chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{200\ mV}{R_{ISENSE}} \quad (1)$$

Example:

If a 1-Ω sense resistor is used, the chopping current will be 200 mV/1 Ω = 200 mA.

Once the chopping current threshold is reached, the H-bridge switches to slow decay mode. Winding current is re-circulated by enabling both of the low-side FETs in the bridge. This state is held until the beginning of the next fixed-frequency PWM cycle.

Note that if current control is not needed, the xISEN pins should be connected directly to ground.

nSLEEP Operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (up to 1 ms) needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (VM). It is recommended to use a pullup resistor when this is done. This resistor limits the current to the input in case VM is higher than 6.5 V. Internally, the nSLEEP pin has a 500-kΩ resistor to GND. It also has a clamping zener diode that clamps the voltage at the pin at 6.5 V. Currents greater than 250 µA can cause damage to the input structure. Hence the recommended pullup resistor would be between 20 kΩ and 75 kΩ.

Protection Circuits

The DRV8833 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will be re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

Overcurrent conditions are detected independently on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, so functions even without presence of the xISEN resistors.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT is driven low in the event of an undervoltage condition.

APPLICATIONS INFORMATION

Parallel Mode

The two H-bridges in the DRV8833 can be connected in parallel for double the current of a single H-bridge. The internal dead time in the DRV8833 prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. The drawing below shows the connections.

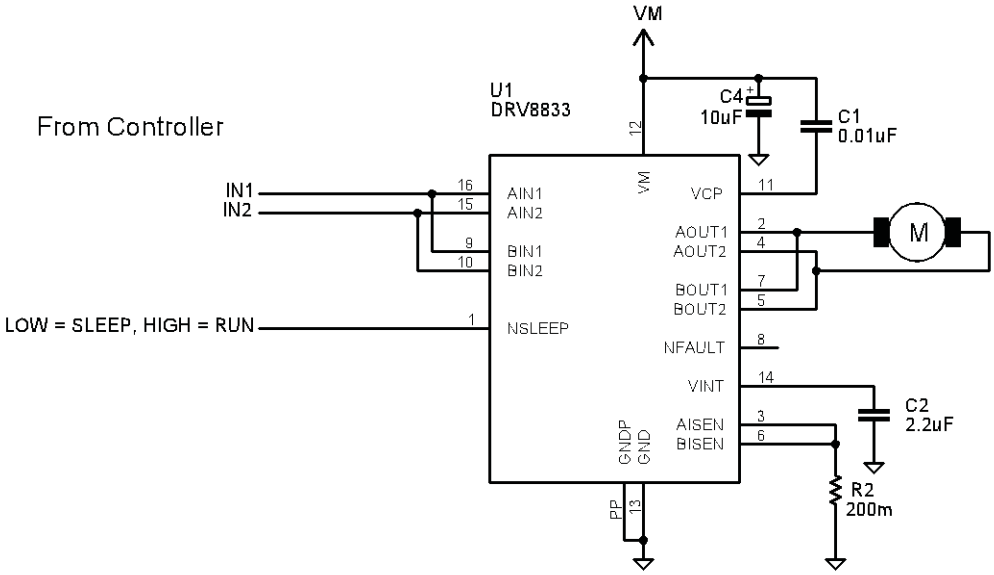


Figure 3. Parallel Mode

THERMAL INFORMATION

Maximum Output Current

In actual operation, the maximum output current achievable with a motor driver is a function of die temperature. This in turn is greatly affected by ambient temperature and PCB design. Basically, the maximum motor current will be the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to stay out of thermal shutdown.

The dissipation ratings given in the datasheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected to be possible without entering thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed via measurement or thermal simulation.

Thermal Protection

The DRV8833 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops by 45°C.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8833 is dominated by the DC power dissipated in the output FET resistance, or RDS(ON). There is additional power dissipated due to PWM switching losses, which are dependent on PWM frequency, rise and fall times, and VM supply voltages. These switching losses are typically on the order of 10% to 30% of the DC power dissipation.

The DC power dissipation of one H-bridge can be roughly estimated by Equation 2.

$$P_{TOT} = (HS\text{ - }R_{DS(ON)} \bullet I_{OUT(RMS)}^{2}) + (LS\text{ - }R_{DS(ON)} \bullet I_{OUT(RMS)}^{2}) \quad (2)$$

where P_{TOT} is the total power dissipation, HS - $R_{DS(ON)}$ is the resistance of the high side FET, LS - $R_{DS(ON)}$ is the resistance of the low side FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to the motor.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ packages (PWP and RTY) use an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

It is important to note that the PW package option is not thermally enhanced and it is recommended to adhere to the power dissipation limits.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8833PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8833PW	Samples
DRV8833PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8833PW	Samples
DRV8833RTYR	ACTIVE	QFN	RTY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833RTYT	ACTIVE	QFN	RTY	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

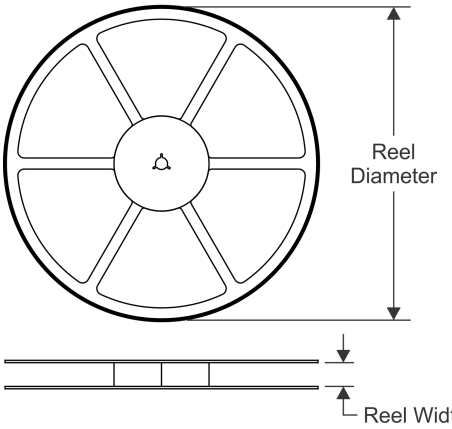
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

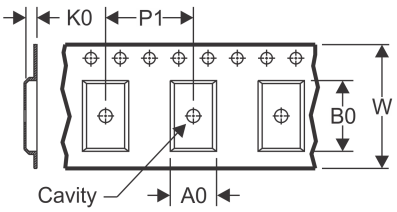
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

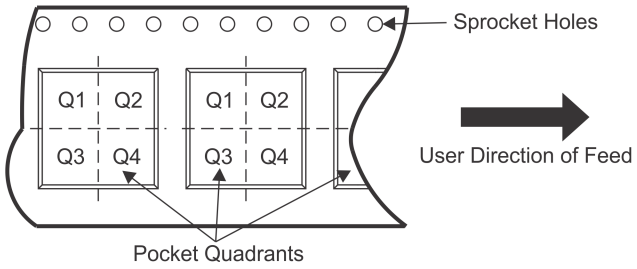


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

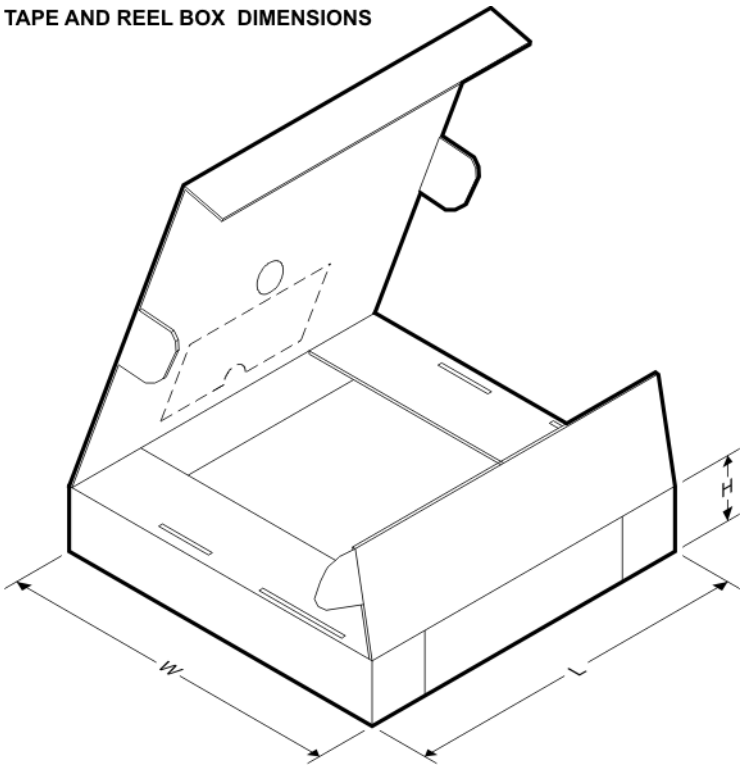
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8833PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8833PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8833RTYR	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8833RTYT	QFN	RTY	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

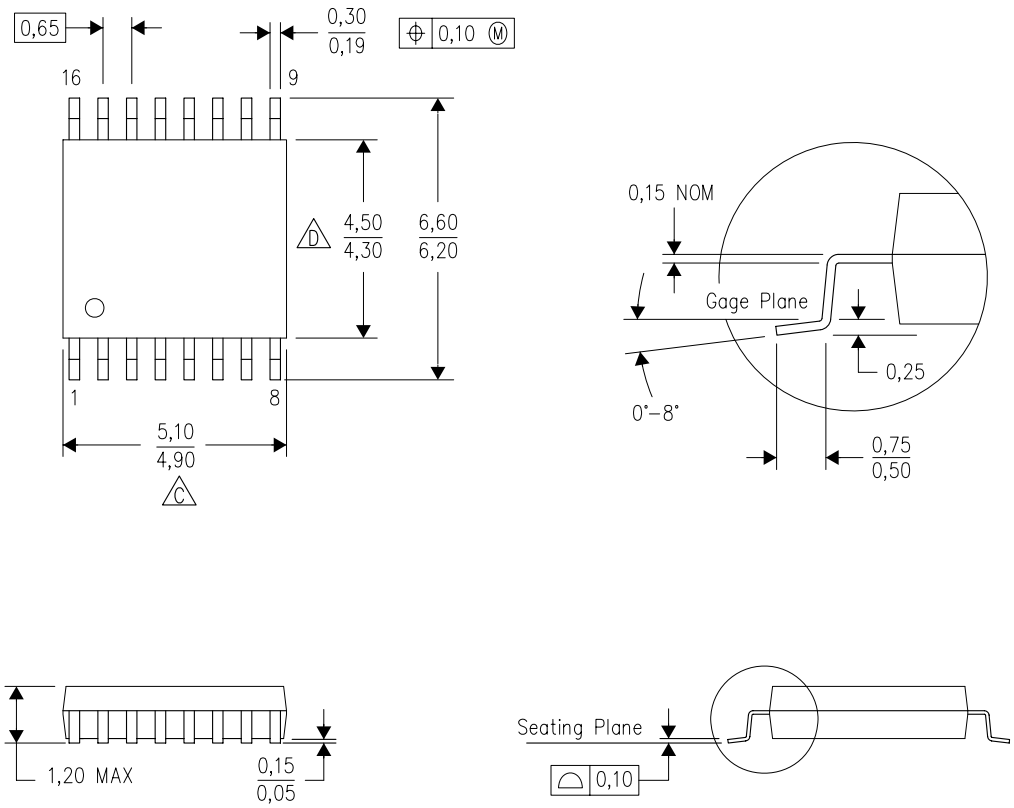
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8833PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
DRV8833PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
DRV8833RTYR	QFN	RTY	16	3000	367.0	367.0	35.0
DRV8833RTYT	QFN	RTY	16	250	210.0	185.0	35.0

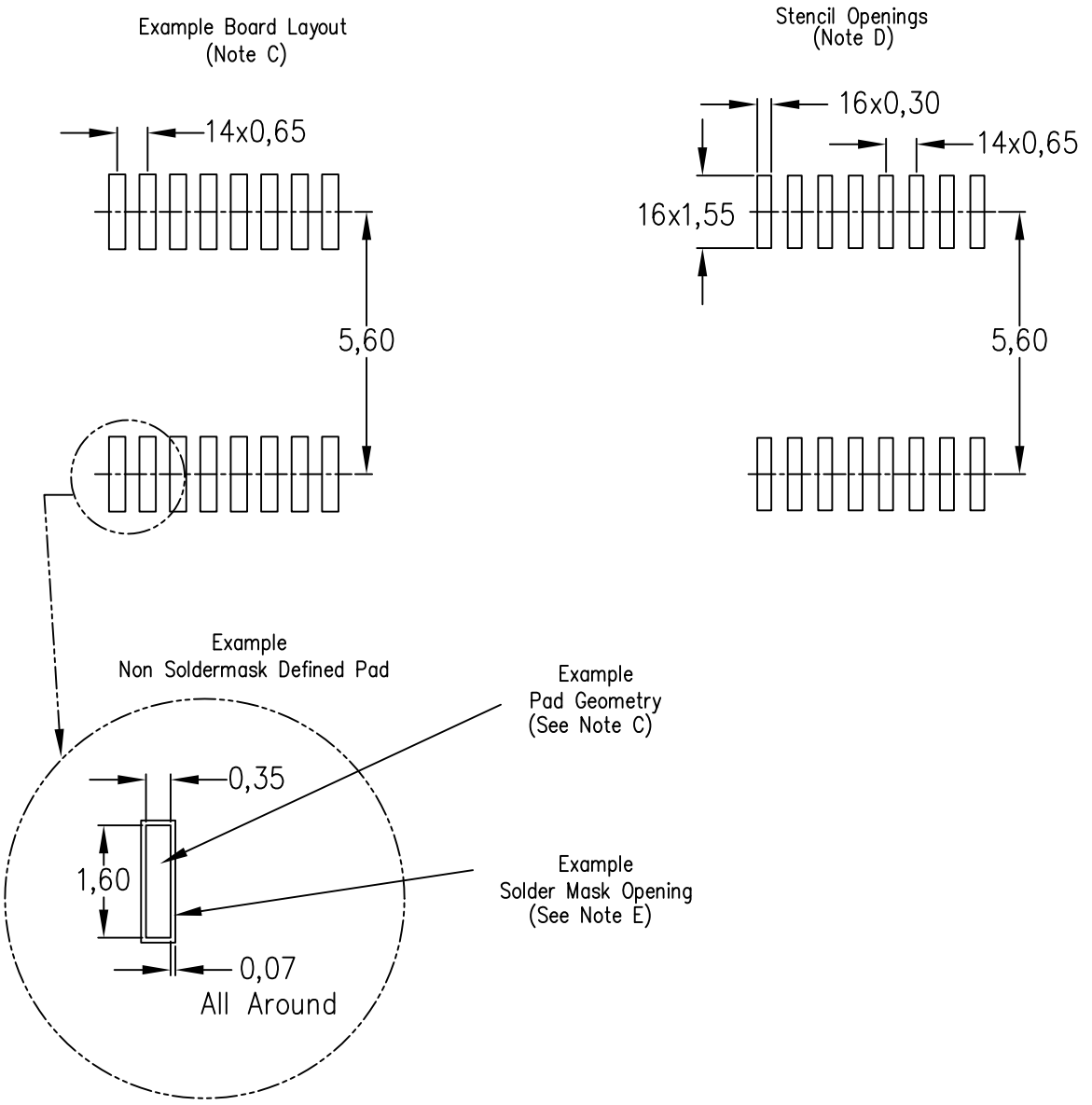
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

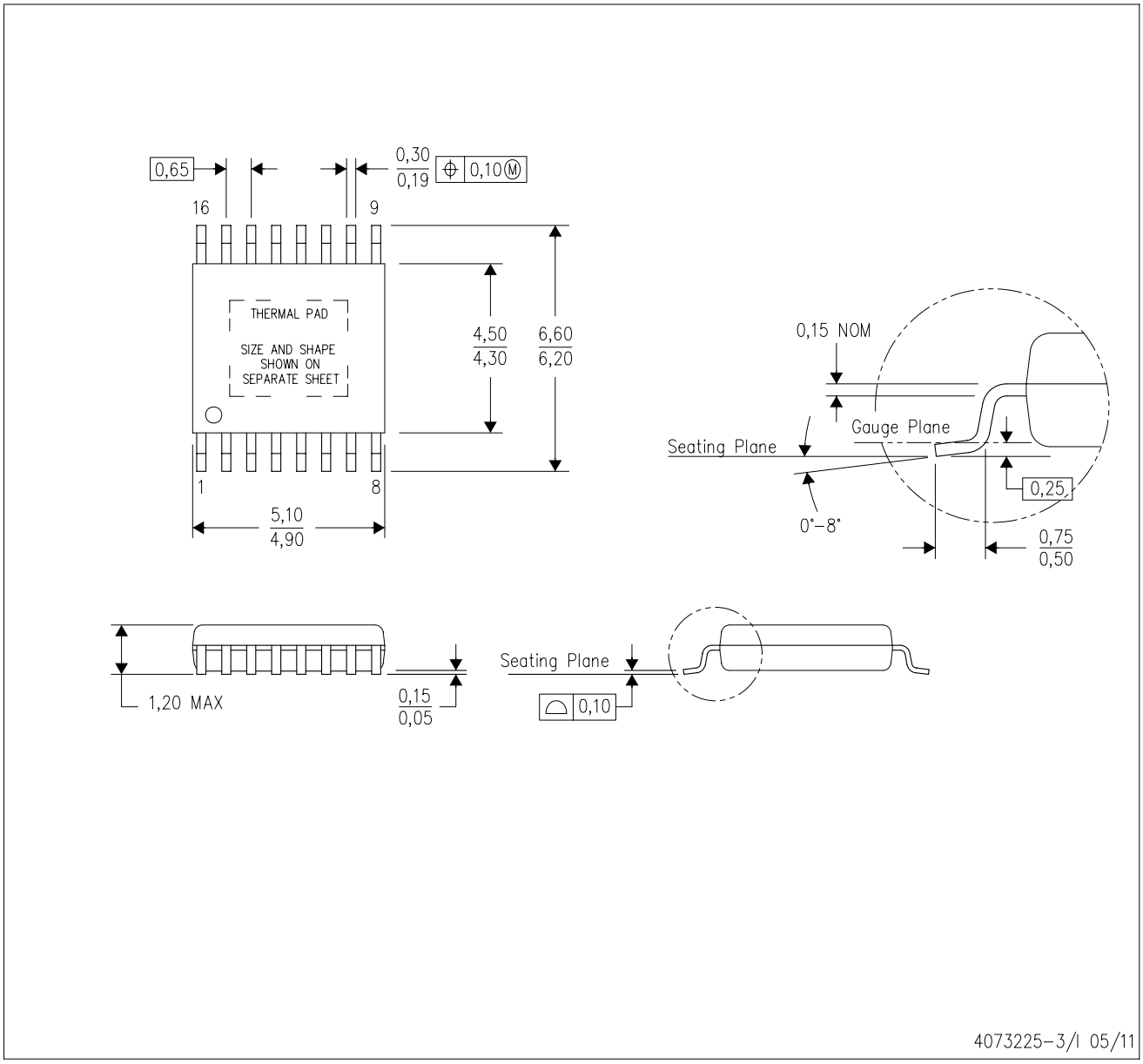
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

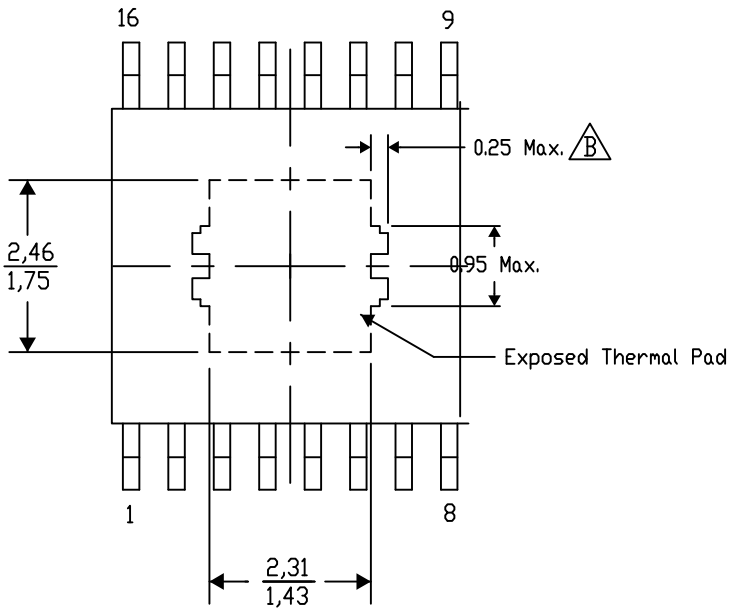
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

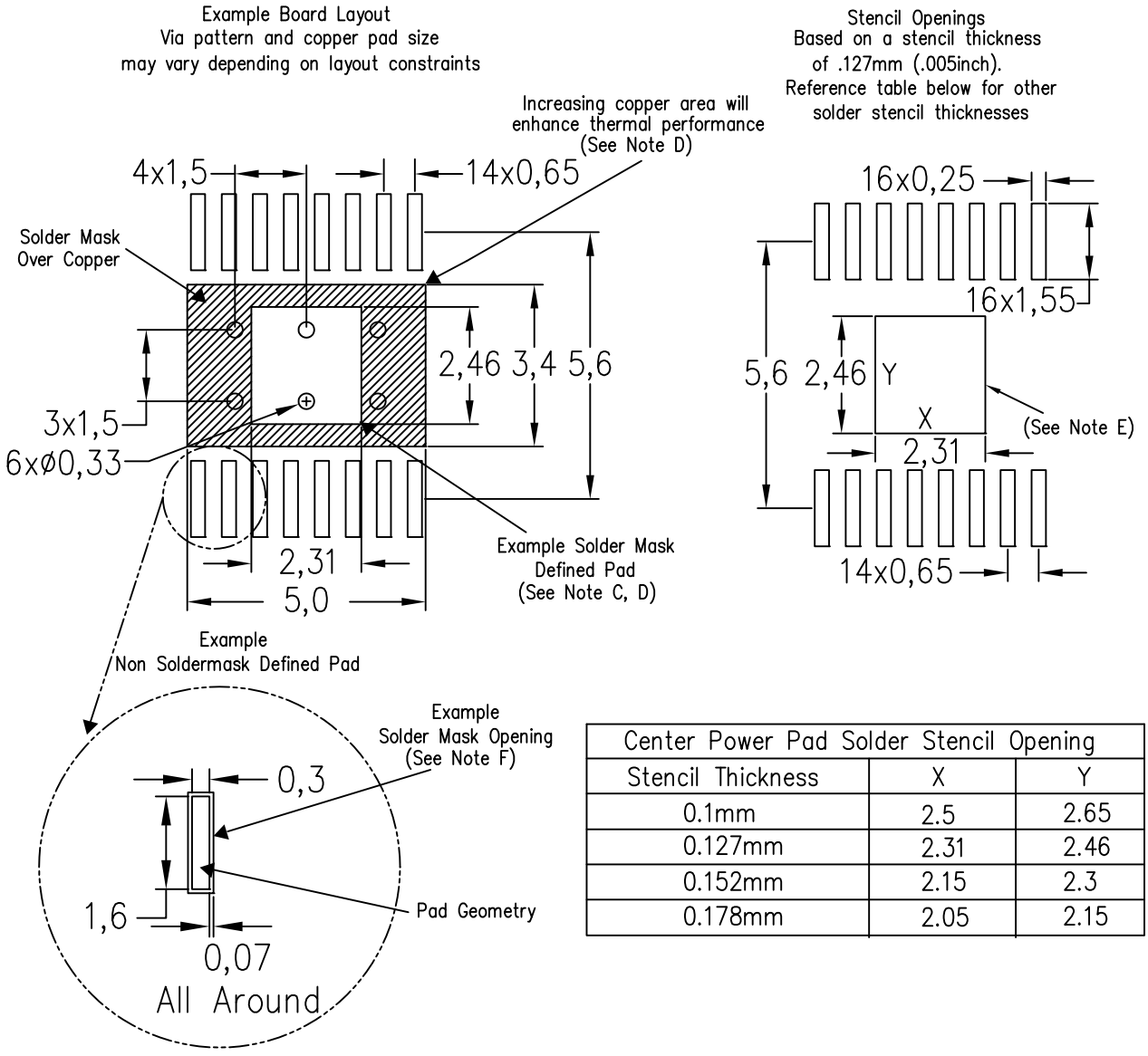
4206332–6/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE

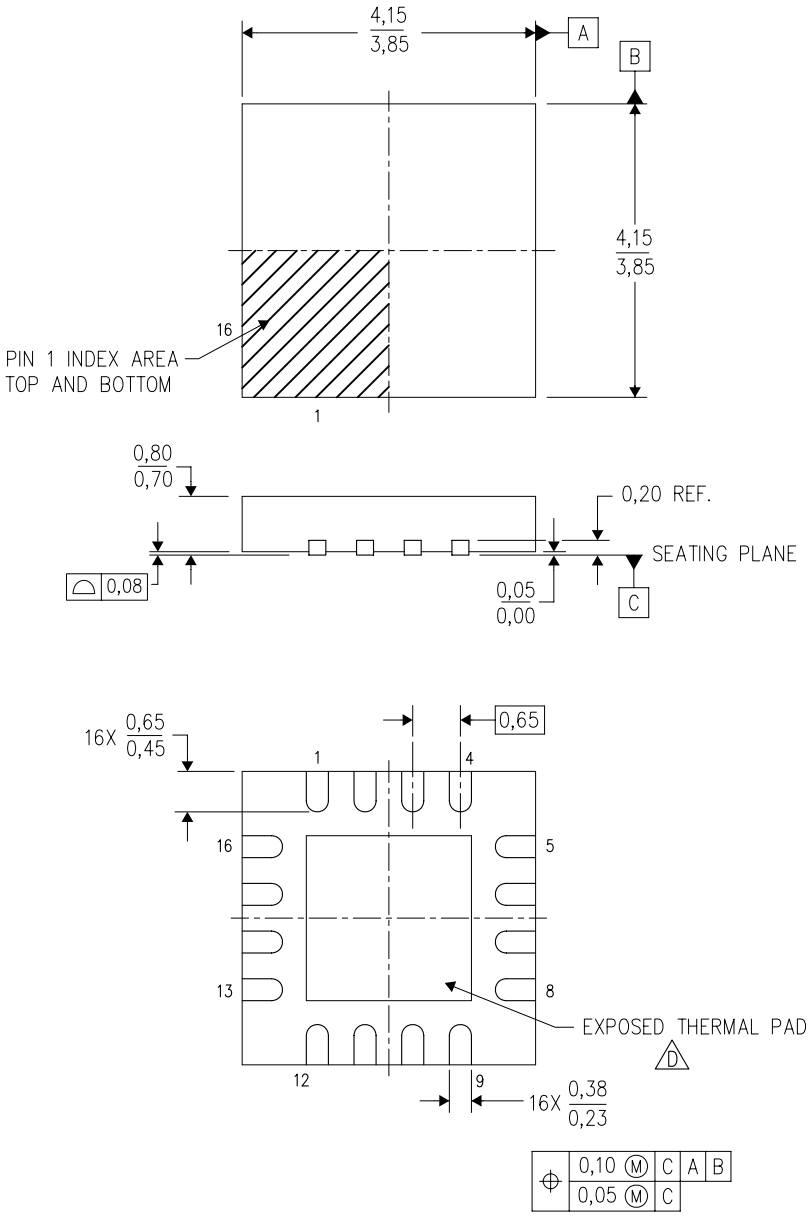


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–3/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4206276/B 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

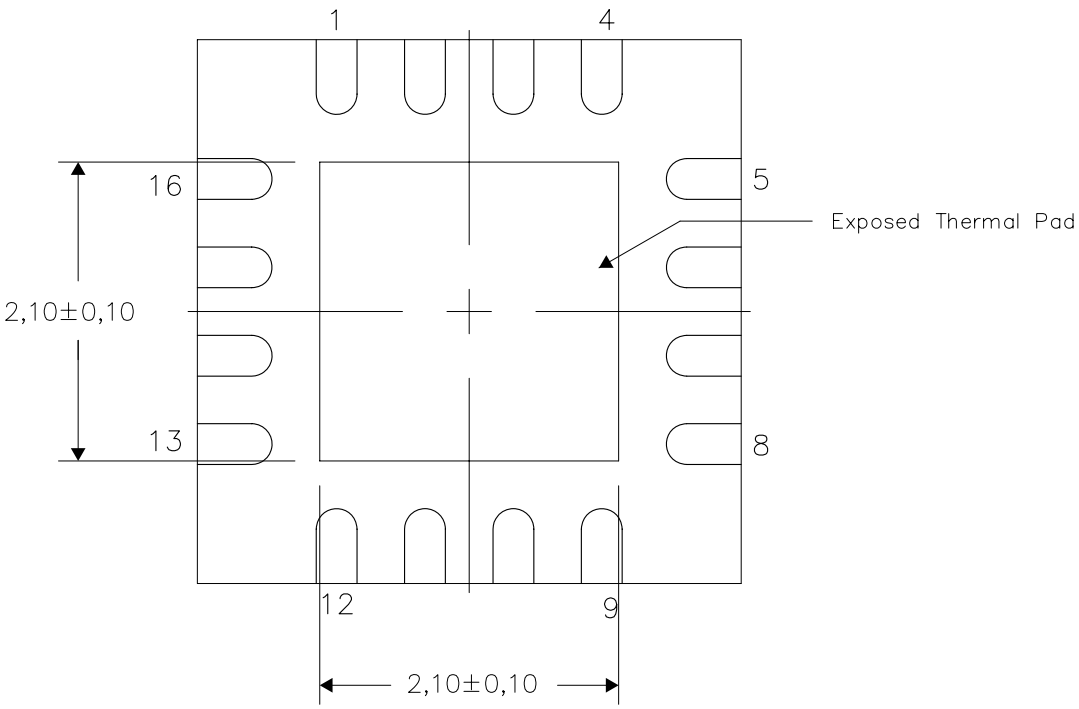
RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



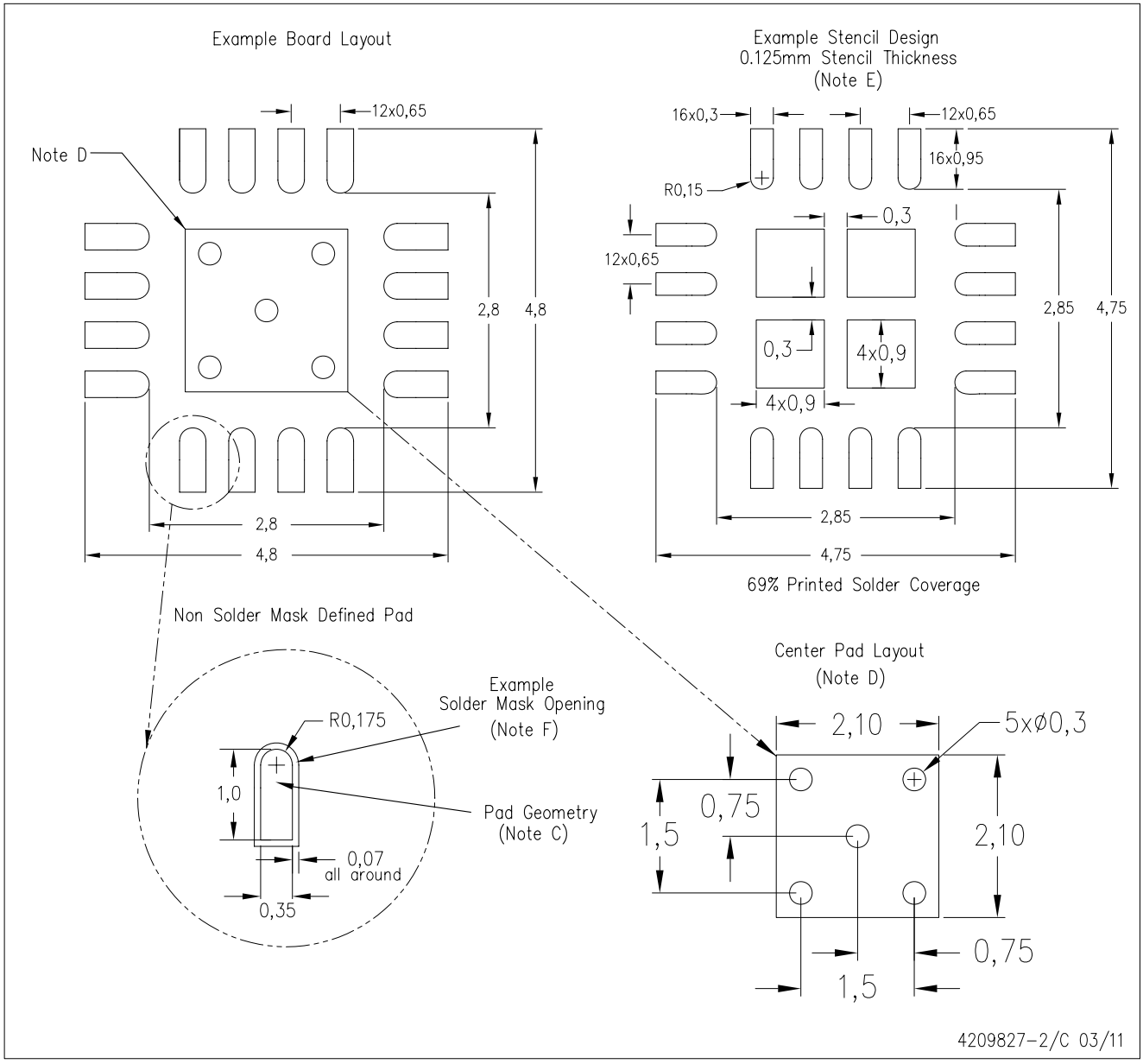
Bottom View

Exposed Thermal Pad Dimensions

4206277–2/E 03/11

NOTE: A. All linear dimensions are in millimeters

RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265